IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:	)	
	)	
Zohar Bogin	)	
	)	
Serial No.: 10/762,037	)	Art Unit: 2182
	)	
Filed: January 20, 2004	)	
	)	Examiner: Sun, Scott C.
For: A Method and An Apparatus to Manage Memory Access Requests	)	
	)	
	)	
	)	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

APPEAL BRIEF UNDER 37 CFR § 41.37

Sir:

Applicants (hereafter "Appellants") hereby submit this Brief in support of its appeal from a final decision by the Examiner, mailed July 24, 2007 in the above-captioned case. Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052-8119.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences that are related to, will directly affect, will be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF THE CLAIMS

Claims 1 and 3-7 are currently pending in this application. Claims 2 and 8-20 have been cancelled. Claims 21-29 have been withdrawn. No claims have been allowed. All pending claims were rejected in the final Office action mailed July 24, 2007 and are the subject of this appeal.

Claims 1, 3, and 13 stand rejected under 35 U.S.C. §102(e) as anticipated.

The remaining claims stand rejected as obvious, but these rejections rely on the anticipation rejection.

Claims 4, 8, 10, and 14-20 stand rejected under 35 U.S.C. §103(a) as obvious.

Claims 5, 6, 11, and 12 stand rejected under 35 U.S.C. §103(a) as obvious.

Claims 7 stands rejected under 35 U.S.C. §103(a) as obvious.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on July 24, 2007, rejecting claims 1, 3-8, and 10-20, Appellants timely filed a Notice of Appeal on October 15, 2007. Claims 8-12 are cancelled.

A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1 refers to a method with the following elements:

dynamically modifying one or more attributes of each of a plurality of requests to access one or more memory devices, wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests (FIG. 1, item 120 and [0023]-[0024]); and

arbitrating among the plurality of requests to select a request to send to the one or more memory devices in a time slot based on the one or more attributes (FIG. 1, item 130 and [0025]).

Independent claim 1 is directed to a novel mechanism for prioritizing requests with different latency sensitivity levels and managing the requests in response to their latency sensitivity. Thus, requests with a high level of latency sensitivity may be sent to the memory devices in a more timely fashion.

VI. GROUNDS OF REJECTION

A. Whether the reference, having no indication of dynamically modifying one or attributes of each of a plurality of requests anticipates the specific limitation of "dynamically modifying one or more attributes of each of a plurality of requests to access one or more memory devices, wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests" under 35 U.S.C. §102(e).

VII. ARGUMENT

A. Introduction

While the arguments below are directed only to Claim 1, they are believed to apply also to the other pending claims.

B. Absent any Teaching of dynamically modifying one or more attributes of each of a plurality of requests, the cited reference cannot anticipate "dynamically modifying one or more attributes of each of a plurality of requests to access one or more memory devices, wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests" as Recited in Claim 1.

The Examiner has rejected claims 1, 3, and 13 under 35 U.S.C. §102 (e) as being anticipated by Morris, U.S. Patent Application No. 2003/0177296 (*Kurth*). Claim 13 has been cancelled and, thus, the rejection of claim 13 is moot.

Regarding the claim terms directed to "dynamically modifying one or more attributes of each of a plurality of requests … wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests," the Office action directs the Appellant's attention to FIG. 4 of *Kurth*. In particular, the Office action directs the Appellant's attention to process block 400 of *Kurth*. The Appellant respectfully notes, however, that FIG. 4 of *Kurth* is directed to a process that includes selecting "a priority level from [a] configuration register" (see, e.g., [0021], lines 3-4) and "[a]fter selecting the priority level, the agent makes 402 the priority request to the arbiter" (see, e.g., [0021], lines 6-8). Thus, the passage relied upon by the Office action does not teach "dynamically modifying one or more attributes of each of a plurality of requests to access one or more memory devices, wherein dynamically modifying the one or more attributes

comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests." Instead, it merely teaches selecting a priority level from a configuration register and sending a priority request to an arbiter that indicates the selected priority level.

Accordingly Claim 1 is believed to be allowable over *Kurth*. The remaining claims are believed to be allowable also on similar grounds and for the particular recitations set forth expressly in each claim, respectively.

Claims 4, 8, 10, and 14-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kurth in* view of Patent Application No. 20030210710 (*Odman*). Claims 8, 10, and 14-20 have been cancelled and, thus, the rejection of claims 8, 10, and 14-20 is moot. For at least the reasons sets forth below, the Appellant submits that claim 4 is not rendered obvious by *Kurth in* view of *Odman*.

Odman is cited as teaching "combining multiple requests … into a larger request … to fill a given time slot." Whether or not *Odman* discloses the limitations cited by the Office action, it does not teach or suggest "dynamically modifying one or more attributes of each of a plurality of requests … wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests," as recited in claim 1. Because neither *Kurth* nor *Odman* teach or suggest the above-cited claim limitations, no combination of *Kurth* and *Odman* teaches or suggests the invention as claimed in claim 1. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Appellant respectfully submits that dependent claim 4 is not rendered obvious by *Kurth* in view of *Odman*.

Dependent claims 5, 6, 11 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kurth in* view of Appellant's Admitted Prior Art (*AAPA*). Claims 5 and 6 depend from claim 1. Claims 11 and 12 have been cancelled and, thus, the rejection of claims 11 and 12 is moot. For at least the reasons sets forth below, the Appellant submits that claims 5, 6, 11, and 12 are not rendered obvious by *Kurth in* view of *AAPA*.

AAPA is cited as teaching "request types." Whether or not *AAPA* discloses the limitations cited by the Office action, it does not teach or suggest "dynamically modifying one or more attributes of each of a plurality of requests … wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests," as recited in claim 1. Because neither *Kurth* nor *AAPA* teach or suggest the above-cited claim limitations, no combination of *Kurth* and *AAPA* teaches or suggests the invention as claimed in claim 1. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Appellant respectfully submits that dependent claims 5 and 6 are not rendered obvious by *Kurth* in view of *AAPA*.

Dependent claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kurth* in view of U.S. Patent Application 2002/0116555 (*Somers*). Claim 7 depends from claim 1. For at least the reasons sets forth below, the Appellant submits that claim 7 is not rendered obvious by *Kurth* in view of *Somers*.

Somers is cited as teaching "plurality of DMA controllers." Whether or not *Somers* discloses the limitations cited by the Office action, it does not teach or suggest "dynamically modifying one or more attributes of each of a plurality of requests … wherein dynamically modifying the one or more attributes comprises dynamically

prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests," as recited in claim 1. Because neither *Kurth* nor *Somers* teach or suggest the above-cited claim limitations, no combination of *Kurth* and *Somers* teaches or suggests the invention as claimed in claim 1. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Appellant respectfully submits that dependent claim 7 is not rendered obvious by *Kurth* in view of *Somers*.

VIII. CONCLUSION

Appellants respectfully submit that all the appealed claims in this application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

Respectfully submitted,

Date: February 15, 2008

/Philip A. Pedigo/Reg. N0. 52,107/
Philip A. Pedigo
Reg. No. 52,107
Attorney for Intel Corporation

Intel Corporation
c/o Intellevate, LLC
P.O. Box 52050
Minneapolis, MN 55402
Tele – (503) 712-5560
Fax – (503) 264-1729

APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(7))

1. (Previously Presented) A method comprising:

dynamically modifying one or more attributes of each of a plurality of requests to access one or more memory devices, wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests; and

arbitrating among the plurality of requests to select a request to send to the one or more memory devices in a time slot based on the one or more attributes.

2. (Cancelled) The method of claim 1, wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests.

3. (Original) The method of claim 2, wherein the latency sensitivity of each of the plurality of requests changes in response to space available in a buffer storing the corresponding request.

4. (Original) The method of claim 1, further comprising dynamically changing a length of each of the plurality of requests in response to a size of the time slot.

5. (Original) The method of claim 1, wherein the plurality of requests comprises one or more data read requests, one or more data write requests, and one or more buffer descriptor read requests.

6. (Original) The method of claim 1, further comprising sending the selected request to the memory devices via a digital multimedia interconnect.

7. (Original) The method of claim 1, further comprising asserting the plurality of requests using a plurality of direct memory access (DMA) controllers in response to an instruction from a processor.

Claims 8-20 (Cancelled)

21. Withdrawn) A system comprising:

a plurality of dynamic random access memory (DRAM) devices;

one or more audio coder-decoders; and

an input/output controller, coupled between the DRAM devices and the one or more audio coder-decoders, the input/output controller having an audio controller, the audio controller comprising

a plurality of memory access controllers to assert a plurality of requests to access one or more of the DRAM devices, wherein one or more attributes of the plurality of requests are dynamically changeable; and

a first arbiter to arbitrate among the plurality of requests to select a request based on the one or more attributes of the plurality of requests.

22. (Withdrawn) The system of claim 21, wherein each of the plurality of memory access controllers further comprises a buffer to temporarily store one or more requests, a priority state machine to dynamically prioritize the one or more requests, and request length determination circuitry to determine length of the one or more requests.

23. (Withdrawn) The system of claim 22, wherein the request length determination circuitry comprises:

a plurality of multiplexers; and

one or more flip-flops coupled to the plurality of multiplexers.

24. (Withdrawn) The system of claim 21, wherein the first arbiter comprises a first plurality of arbiters and a second arbiter, outputs of the first plurality of arbiters are coupled to inputs of the second arbiter.

25. (Withdrawn) The system of claim 24, wherein the first plurality of arbiters comprise a plurality of First Come First Serve (FCFS) arbiters.

26. (Withdrawn) The system of claim 24, wherein the second arbiter comprises a fixed priority arbiter.

27. (Withdrawn) The system of claim 22, wherein the priority state machine prioritizes the plurality of requests based on space available in the buffer of each of the plurality of memory access controllers.

28. (Withdrawn) The system of claim 21, further comprising:

a memory controller coupled to the DRAM devices; and

a digital multimedia interconnect, coupled between the memory controller and the input/output controller, wherein the selected request is sent to one or more of the DRAM devices via the digital multimedia interconnect and the memory controller.

29. (Withdrawn) The system of claim 28, further comprising a central processing unit, coupled to the memory controller, to send an instruction to the input/output controller to cause the plurality of memory access controllers to assert the plurality of requests.

XI. EVIDENCE APPENDIX

None.

XII. RELATED PROCEEDINGS APPENDIX

None.